OTA-Based High Frequency CMOS Multiplier and Squaring Circuit

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***Abstract*- A gigahertz analog multiplier based on OTA and squaring is proposed. The multiplier has gigahertz frequency response is suitable to use in communication system. The circuit is based on 0.18 µm CMOS technology simulated using PSPICE level 7. This technique provides; wide dynamic range, GHz-bandwidth response and low power consumption. The proposed circuit has been simulated with PSPICE and achieved -3dB bandwidth of 3.96GHz. The total power dissipation is 0.588mW with ±1V power supply voltages..**

I. INTRODUCTION

An analog multiplier is an importance basic building block for the design of analog nonlinear function circuits. It is found application in, for examples, automatic gain control, frequency translation, waveform generation, linear modulation, neural networks, and other signal processing circuits. Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in bipolar and CMOS technologies [1, 2]. The other approaches in CMOS technology are based on square-law characteristics of MOS transistor which are biased in saturation region [3, 4, 5] and that based on the current-voltage characteristics of MOS transistor in the nonsaturation region [6]. However, all mention techniques require resistors to obtain the output signal in voltage form. The use of resistors may require external resistors, or occupy large chip area to implement in IC form and also cause of the multiplier frequency degradation.

This paper proposes a multiplier that uses operational transconductance amplifiers (OTA's) CMOS combining with squaring circuits to get the quarter square algebraic identity.

II. CIRCUIT DESCRIPTION

The principle of the proposed multiplier is based on the quarter-square algebraic identity, that is $(V_1+V_2)^2-(V_1-V_2)^2=4V_1V_2$. Therefore, the circuit needs summing, and squarer circuits. The summation and subtraction between two input voltages are firstly performed, then, the results are squared. Finally, the multiplication is obtained by subtracting the square of the difference from the square of the sum. The principles of the squaring circuit and the simple OTA circuit as a differential amplifier are described in the next subsection.

A. Squaring Circuit

Considering the circuit in Fig. 1, while both transistor work in saturation region, the currents through the transistors can be expressed as,

$$I_1=\frac{K_1}{2}(V_{GS1}-V_{TH1})^2$$
$$I_2=\frac{K_2}{2}(V_{GS2}-V_{TH2})^2 \quad (1)$$
$$V_{GS}>V_{TH},\ V_{DS}\geq V_{GS}-V_{TH}$$

where $K=\mu_0 C_{ox}(W/L)$ is the parameter of transistor, μ_O is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage and V_{TH} is threshold voltage of the MOS transistor. Suppose all transistors are homogeneous, then $K_1=K_2=K$ and $V_{TH1}=V_{TH2}=V_{TH}$, then the summation of I_1+I_2 is

$$I_1+I_2=\frac{K}{2}\left[(+V_{in}-V_A-V_{TH1})^2+(-V_{in}-V_A-V_{TH1})^2\right] \quad (2)$$

It can be derived from (2) that,

$$I_{sum}=\frac{K\left(V_{in}^4+2V_{in}^2(V_{SS}+2V_{TH})^2+(V_{SS}+2V_{TH})^4\right)}{4(V_{SS}+2V_{TH})^2} \quad (3)$$

For small signal of V_{in}, and it can be assumed that $V_{in}^4\approx 0$. Then, the output current can be expressed as the simple input signal squarer as follows,

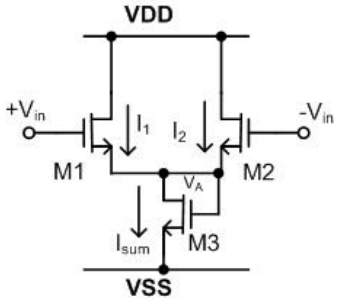

Fig. 1. Squaring Circuit

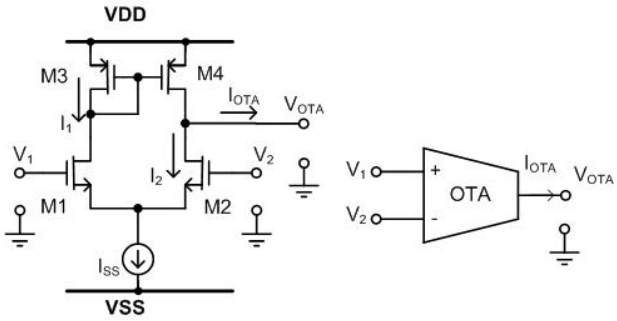

Fig. 2. OTA circuit and its symbol

$$I_{sum} = \frac{K}{2}V_{in}^2 + \frac{K}{4}\left(V_{SS} + 2V_{TH}\right)^2 \quad (4)$$

The voltage at V_A can be derived from (4) using small signal model that is

$$V_A = \frac{K}{2g_m}V_{in}^2 + \frac{K}{4g_m}\left(V_{SS} + 2V_{TH}\right)^2 \quad (5)$$

B. OTA circuit

Fig. 2 shows the simple CMOS OTA circuit that consists of source coupled n-channel MOSFET. It can also be considered as an active mirror circuit. I_{SS} consists of $I_1 + I_2$. The circuit in Fig. 2 shows that NMOS M1 and M2 provide amplification, while PMOS M3 and M4 are used as an active load configuration.

The mathematical analysis gives the expression of the output current as follows;

$$\left(I_1 - I_2\right)^2 = K^2\left(\Delta V\right)^2\left(\frac{I_{SS}}{K} - \frac{\left(\Delta V\right)^2}{4}\right)$$

Or
$$\left(I_1 - I_2\right) = K\left(\Delta V\right)\sqrt{\left(\frac{I_{SS}}{K} - \frac{\left(\Delta V\right)^2}{4}\right)} \quad (6)$$

For small signal of ΔV, it can be assumed that $\Delta V^2 \approx 0$. Then the difference of output current, $(I_1 - I_2) = I_{OTA}$ and can be expressed as

$$I_{OTA} = g_m\left(\Delta V\right) \quad (7)$$

where $g_m = \sqrt{I_{SS}K}$, $K = \mu_0 C_{ox}\left(W/L\right)$.

C. The Proposed Circuit

The principle of the proposed multiplier is based on the quarter-square algebraic identity, that is $\left(V_1 + V_2\right)^2 - \left(V_1 - V_2\right)^2 = 4V_1V_2$. Employ the squaring circuit of Fig. 1 and the OTA circuit of Fig. 2, the analog multiplier can be realized as shown in Fig. 3.

The sum and difference outputs from these stages are applied to the squarer circuits formed by *M*31-*M33* for summing and *M*34-*M*36 for difference, and the squarer outputs are through M33 and M36. The subtraction between squarer summing and squarer difference gives the result of multiplier in voltage mode. Fig. 3, transistors M17-M24 act as R_{eq} to convert the output current of OTA to be voltage. R_{eq} has expression as

$$R_{eq} = \frac{1}{4K\left(V_{DD} - V_{TH}\right)} \quad (8)$$

From (4), (7) and (8), the results of multiplier V_{out} can be expressed as

$$V_{out} = \frac{K}{2g_m}\left(V_{sum}^2 - V_{sub}^2\right) \quad (9)$$

$$V_{out} = \frac{K.g_m R_{eq}^2}{2}\left(\left(V_x + V_y\right)^2 - \left(V_x - V_y\right)^2\right)$$

$$V_{out} = C\,.V_x V_y \quad (10)$$

where $C = 2K.g_m R_{eq}^2$, V_{out} is the voltage that through the transistor.

III. Simulation Results

The performance of the proposed analog multiplier circuit is simulated using PSPICE with level 7 model of 0.18µm MOS parameter from MOSIS [7]. The complete circuit of the multiplier is shown in Fig. 3, and the simulation uses 0.18µm CMOS with L/W = 0.27/0.27 (µm), the supply voltage V_{DD} = +1V and V_{SS} = -1V. Since the drains of all squarer transistors (M31, M32, M34, and M35) are connected to V_{DD}, they must work on the saturation region. Set V_x and V_y between -100mV to and +100mV, M1 M2 and M4 become work in saturation region, so that the circuit will work as multiplier as in (10).

A. DC Sweep Analysis

Fig. 4 shows the DC transfer characteristics of the proposed analog multiplier without any load. The output voltage swings between -16mV and +16mV for the input voltage range of ±100mV. It should be note that nonlinear graph is smoothly seen especially in the edge of the graph. It may due to the non linearity effect as shown in (3) and (6). If the smaller signal is taken, then the more linear graph can be received.

B. AC Analysis

The simplified model is used in order to estimate the frequency response of the OTA. Replace V_{in}, M1, and M2 by a Thevenin equivalent gives the transfer function of the circuit in Fig. 2, and can be derived as in (11) or (12) [8].

Meanwhile, the squaring circuit is considered as a source follower for the frequency response analysis. The frequency response of the source follower is determined by two capacitances designated as C_1 and C_2. C_1 consists of capacitances connected between the input and output of the source follower, which are primarily C_{gs1}. C_2 consists of capacitances connected from the output of the source follower to ground'. It includes C_{gd2} (or C_{gs2}), C_{bd2}, C_{bs1}. The *g, d, s, and b* notations correspond to the gate, drain, source and bulk of the transistor. The small-signal frequency response can be written as [9]

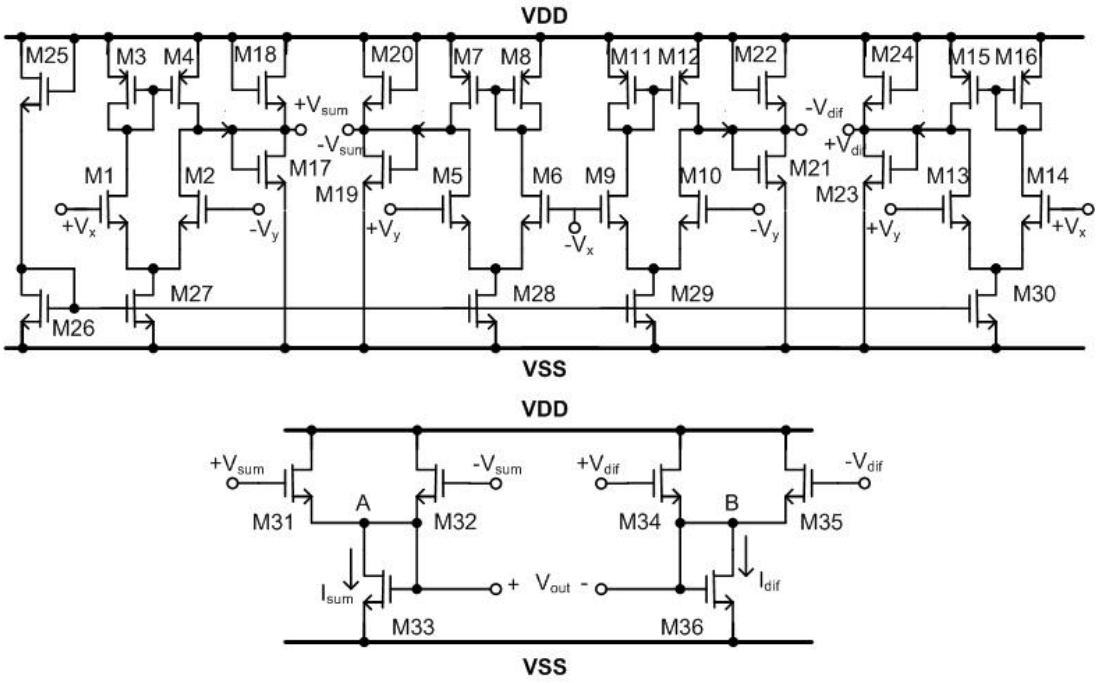

Fig. 3. The proposed of analog multiplier circuit

$$\frac{V_{out}}{V_{in}} = \frac{g_{mN} r_{oN} \left(2g_{mP} + sC_E\right)}{2r_{oP} r_{oN} C_E C_L s^2 + \left[\left(2r_{oN} + r_{oP}\right)C_E + r_{oP}\left(1 + g_{mP} r_{oN}\right)C_L\right]s + 2g_{mP}\left(r_{oN} + r_{oP}\right)} \tag{11}$$

or

$$\frac{V_{out}}{V_{in}} = \frac{\left(a_0 + a_1 s\right)}{b_2 s^2 + b_1 s + b_0} \tag{12}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} + sC_1}{gds1 + gds2 + gm1 + gm2 + GL + s\left(C_1 + C_2\right)} \tag{13}$$

$$\frac{V_{out}}{V_{in}} = \frac{c_0 + c_1 s}{d_0 + d_1 s} \tag{14}$$

Since the circuit consists of OTA and squaring, then the transfer function is the multiplication of (12) and (14) and can be expressed as

$$\frac{V_{out}}{V_{in}} = \left(\frac{a_0 + a_1 s}{b_2 s^2 + b_1 s + b_0}\right)\left(\frac{c_0 + c_1 s}{d_0 + d_1 s}\right) \tag{15}$$

$$\frac{V_{out}}{V_{in}} = \frac{p_0 + p_1 s + p_2 s^2}{q_0 + q_1 s + q_2 s^2 + q_3 s^3} \tag{16}$$

Fig. 5 shows the frequency response of the multiplier. For the frequency characteristic of the multiplier, a dc voltage is applied to V_y while V_x is the variable frequency. From the result, the -3dB bandwidth of 3.96GHz is achieved.

C. Transient Analysis

Fig. 6 shows the transient analysis of the multiplier as amplitude modulator. The modulation is performed when the input voltage V_x and V_y are respectively 1.6GHz and 100MHz sinusoidal input signals with peak amplitude of 0.1V.

Table I shows the performances of the multiplier. The multiplier has GHz-bandwidth response with low power consumption. The circuit has supply voltage ± 1 V and the power dissipation 0.588mW. The proposed circuit has achieved -3dB bandwidth of 3.96GHz.

IV. CONCLUSION

A voltage-mode four-quadrant analog multiplier based on simple OTA's and squaring circuits is proposed. The circuit is based on the simple square mathematics model that implements simple operational transconductance amplifier pairs and squaring circuit. It achieves the multiplied output signal in voltage form without using resistors. The design uses 0.18µm CMOS process and the performance has been demonstrated by using PSPICE. The circuit has the bandwidth 3.96 GHz.

TABLE I

PERFORMANCE OF THE MULTIPLIER

Number of MOS	36
Supply	± 1 V
W/L	0.27µm/0.27µm
Input range	± 100mV
Output range	± 16mV
-3 dB Freq Response	3.96 GHz
Power dissipation	0.588mW

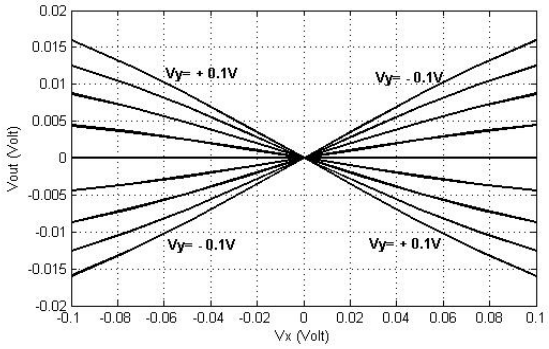

Fig. 4 DC transfer characteristics

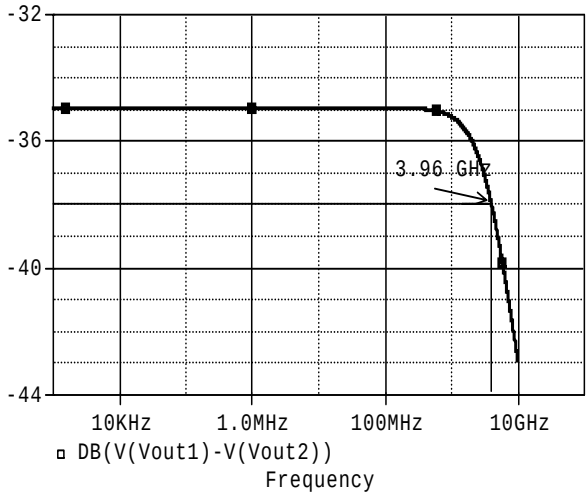

Fig. 5 The frequency response of the multiplier

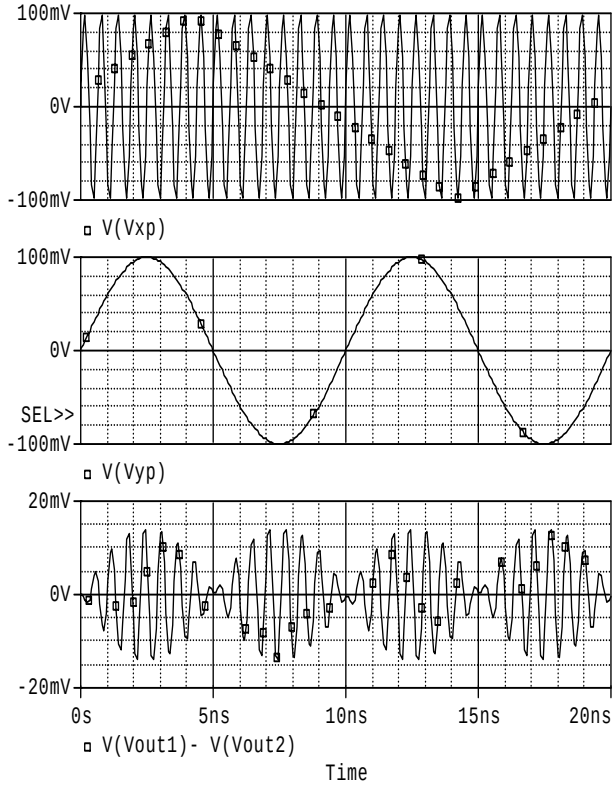

Fig. 6 The transient analysis of the multiplier as an amplitude modulator

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